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| **Symbol** | **Parameter** | **2.5 GT/s** | **5.0 GT/s** | **Unit** | **Comments** |
| **Transmitter Specifications** | | | | | |
| UI | Unit Interval | 399.88  (min)  400.12  (max) | 199.94  (min)  200.06  (max) | ps | The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations. See Note 1. |
| VTX-DIFF-PP | Differential p-p Tx voltage swing | 0.8 (min)  1.2 (max) | 0.8 (min)  1.2 (max) | V | As measured with compliance test load. Defined as 2\*|VTXD+ - VTXD- |. |
| VTX-DIFF-PP-LOW | Low power differential p-p Tx voltage swing | 0.4 (min)  1.2 (max) | 0.4 (min)  1.2 (max) | V | As measured with compliance test load. Defined as 2\*|VTXD+ - VTXD- |. See Note 9. |
| VTX-DE-RATIO-3.5dB | Tx de-emphasis level ratio | 3.0 (min)  4.0 (max) | 3.0 (min)  4.0 (max) | dB | See Note 11 for details. |
| VTX-DE-RATIO-6dB | Tx de-emphasis level | N/A | 5.5 (min)  6.5 (max) | dB | See Note 11 for details |
| TMIN-PULSE | Instantaneous lone pulse width | Not specified | 0.9 (min) | UI | Measured relative to rising/falling pulse. See Notes 2, 10. |
| TTX-EYE | Transmitter Eye including all jitter sources | 0.75 (min) | 0.75 (min) | UI | Does not include SSC or Refclk jitter. Includes Rj at 10-12. See Notes 2, 3, 4, and 10. Note that 2.5 GT/s and 5.0 GT/s use different jitter determination methods. |
| TTX-EYE-MEDIAN-to-MAX-JITTER | Maximum time between the jitter median and max deviation from the median | 0.125 (max) | Not specified | UI | Measured differentially at zero crossing points after applying the 2.5 GT/s clock recovery function. See Note 2. |
| TTX-HF-DJ-DD | Tx deterministic jitter > 1.5 MHz | Not specified | 0.15 (max) | UI | Deterministic jitter only. See Notes 2 and 10. |
| TTX-LF-RMS | Tx RMS jitter < 1.5 MHz | Not specified | 3.0 | ps  RMS | Total energy measured over a 10 kHz –1.5 MHz range. |
| TTX-RISE-FALL | Transmitter rise and fall time | 0.125 (min) | 0.15 (min) | UI | Measured differentially from 20% to 80% of swing. See Note 2. |
| TRF-MISMATCH | Tx rise/fall mismatch | Not specified | 0.1 (max) | UI | Measured from 20% to 80% differentially. See Note 2. |
| BWTX-PLL | Maximum Tx PLL bandwidth | 22 (max) | 16 (max) | MHz | Second order PLL jitter transfer bounding function. See Note 6 |
| BWTX-PLL-LO-3DB | Minimum Tx PLL BW for 3 dB  peaking | 1.5 (min) | 8 (min) | MHz | Second order PLL jitter transfer bounding function. See Notes 6 and 8. |
| BWTX-PLL-LO-1DB | Minimum Tx PLL BW for 1 dB  peaking | Not specified | 5 (min) | MHz | Second order PLL jitter transfer bounding function. See Notes 6 and 8. |
| PKGTX-PLL1 | Tx PLL peaking with 8 MHz min  BW | Not specified | 3.0 (max) | dB | Second order PLL jitter transfer bounding function. See Notes 6 and 8. |
| PKGTX-PLL2 | Tx PLL peaking with 5 MHz min BW | Not specified | 1.0 (max) | dB | See Note 8. |
| RLTX-DIFF | Tx package plus Si differential return loss | 10 (min) | 10 (min) for 0.05 -1.25 GHz  8 (min) for1.25 -2.5 GHz | dB |  |
| RLTX-CM | Tx package plus Si common mode return loss | 6 (min) | 6 (min) | dB | Measured over 0.05 – 1.25 GHz range for 2.5 GT/s and 0.05 – 2.5 GHz range for 5.0 GT/s. (S11 parameter) |
| ZTX-DIFF-DC | DC differential Tx impedance | 80 (min)  120 (max) | 120 (max) | Ω | Low impedance defined during signaling. Parameter is captured for 5.0 GHz by RLTX-DIFF. |
| VTX-CM-AC-PP | Tx AC common mode voltage (5.0 GT/s) | Not specified | 100 (max) | mVPP | See Note 5. |
| VTX-CM-AC-P | Tx AC common mode voltage (2.5 GT/s) | 20 | Not specified | mV | See Note 5. |
| ITX-SHORT | Transmitter short-circuit current limit | 90 (max) | 90 (max) | mA | The total current Transmitter can supply when shorted to ground. |
| VTX-DC-CM | Transmitter DC common-mode voltage | 0 (min)  3.6 (max) | 0 (min)  3.6 (max) | V | The allowed DC common-mode voltage at the Transmitter pins under any conditions |
| VTX-CM-DC-ACTIVEIDLE-DELTA | Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle. | 0 (min)  100 (max) | 0 (min)  100 (max) | mV | |VTX-CM-DC [during L0] – VTX-CM-Idle-DC [during Electrical Idle]|<= 100 mV  VTX-CM-DC = DC(avg) of |VTX-D+ + VTX-D-|/2  VTX-CM-Idle-DC= DC(avg) of |VTX-D+ + VTX-D-|/2  [Electrical Idle] |
| VTX-CM-DC-LINEDELTA | Absolute Delta of DC Common Mode Voltage between D+ and D- | 0 (min)  25 (max) | 0 (min)  25 (max) | mV | |VTX-CM-DC-D+ [during L0] – VTX-CM-DC-D- [during L0.]| ≤ 25mV  VTX-CM-DC-D+ = DC(avg) of |VTX-D+| [during L0]  VTX-CM-DC-D- = DC(avg) of |VTX-D-| [during L0] |
| VTX-IDLE-DIFF-AC-p | Electrical Idle Differential Peak Output Voltage | 0 (min)  20 (max) | 0 (min)  20 (max) | mV | VTX-IDLE-DIFFp = |VTX-Idle-D+ - VTx-Idle-D-| ≤ 20 mV.  Voltage must be high pass filtered to remove any DC component. |
| VTX-IDLE-DIFF-DC | DC Electrical Idle Differential Output Voltage | Not specified | 0 (min)  5 (max) | mV | VTX-IDLE-DIFF-DC = |VTX-Idle-D+ - VTx-Idle-D-| ≤ 5 mV.  Voltage must be low pass filtered to remove any AC component. Filter characteristics complementary to above. |
| VTX-RCV-DETECT | The amount of voltage change allowed during Receiver Detection | 600 (max) | 600 (max) | mV | The total amount of voltage change in a positive direction that a Transmitter can apply to sense whether a low impedance Receiver is present. Note: Receivers display substantially different impedance for VIN <0 vs VIN > 0. |
| TTX-IDLE-MIN | Minimum time spent in Electrical Idle | 20 (min) | 20 (min) | ns | Minimum time a Transmitter must be in Electrical Idle. |
| TTX-IDLE-SET-TOIDLE | Maximum time to transition to a valid Electrical Idle after sending an EIOS | 8 (max) | 8 (max) | ns | After sending the required number of EIOSs, the Transmitter must meet all Electrical Idle specifications within this time. This is measured from the end of the last UI of the last EIOS to the Transmitter in Electrical Idle. |
| TTX-IDLE-TO-DIFFDATA | Maximum time to transition to valid diff signaling after leaving Electrical Idle | 8 (max) | 8 (max) | ns | Maximum time to transition to valid diff signaling after leaving Electrical Idle. This is considered a debounce time to the Tx. |
| TCROSSLINK | Crosslink random timeout | 1.0 (max) | 1.0 (max) | ms | This random timeout helps resolve potential conflicts in the crosslink configuration. |
| LTX-SKEW | Lane-to-Lane Output Skew | 500 ps + 2 UI (max) | 500 ps + 4 UI (max) | ps | Between any two Lanes within a single Transmitter. |
| CTX | AC Coupling Capacitor | 75 (min)  200 (max) | 75 (min)  200 (max) | nF | All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. |
| **Notes** | 1. SSC permits a +0, - 5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.  2. Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of ≥12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0 GT/s must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5 GT/s may be measured within 200 mils of Tx device’s pins, although deconvolution is recommended. At least 106 UI of data must be acquired.  3. Transmitter jitter is measured by driving the Transmitter under test with a low jitter “ideal” clock and connecting the DUT to a reference load.  4. Transmitter raw jitter data must be convolved with a filtering function that represents the worst case CDR tracking BW. 2.5 GT/s and 5.0 GT/s use different filter functions. After the convolution process has been applied, the center of the resulting eye must be determined and used as a reference point for obtaining eye voltage and margins.  5. Measurement is made over at least 106 UI.  6. The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table.  7. Measurements are made for both common mode and differential return loss. The DUT must be powered up and DC isolated, and its data+/data- outputs must be in the low-Z state at a static value  8. A single combination of PLL BW and peaking is specified for 2.5 GT/s implementations. For 5.0 GT/s, two combinations of PLL BW and peaking are specified to permit designers to make a tradeoff between the two parameters. If the PLL's min BW is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's min BW is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met. In both cases, the max PLL BW is 16 MHz.  9. Low swing output, defined by VTX-DIFF-PP-LOW must be implemented with no de-emphasis.  10. For 5.0 GT/s, de-emphasis timing jitter must be removed. An additional HPF function must be applied. This parameter is measured by accumulating a record length of 106 UI while the DUT outputs a compliance pattern. TMIN-PULSE is defined to be nominally 1 UI wide and is bordered on both sides by pulses of the opposite polarity.  11. Root complex Tx de-emphasis is configured from Upstream controller. Downstream Tx de-emphasis is set via a command, issued at 2.5 GT/s. | | | | |
| **Receiver Specifications** | | | | | |
| UI | Unit Interval | 399.88  (min)  400.12  (max) | 199.94  (min)  200.06  (max) | ps | UI does not account for SSC caused variations. |
| VRX-DIFF-PP-CC | Differential Rx peak-peak voltage for common Refclk Rx architecture | 0.175 (min)  1.2 (max) | 0.120 (min)  1.2 (max) | V |  |
| VRX-DIFF-PP-DC | Differential Rx peak-peak voltage for data clocked Rx architecture | 0.175 (min)  1.2 (max) | 0.100 (min)  1.2 (max) | V |  |
| TRX-EYE | Receiver eye time opening | 0.40 (min) | N/A | UI | Minimum eye time at Rx pins to yield a 10-12 BER. See Note 1. |
| TRX-TJ-CC | Max Rx inherent timing error | N/A | 0.40 (max) | UI | Max Rx inherent total timing error for common Refclk Rx architecture. See Note 2. |
| TRX-TJ-DC | Max Rx inherent timing error | N/A | 0.34 (max) | UI | Max Rx inherent total timing error for data clocked Rx architecture. See Note 2. |
| TRX-DJ-DD-CC | Max Rx inherent deterministic timing error | N/A | 0.30 (max) | UI | Max Rx inherent deterministic timing error for common Refclk Rx architecture. See Note 2. |
| TRX-DJ-DD-DC | Max Rx inherent deterministic timing error | N/A | 0.24 (max) | UI | Max Rx inherent deterministic timing error for data clocked Rx architecture. See Note 2. |
| TRX-EYE-MEDIAN-to-MAX-JITTER | Max time delta between median and deviation from median | 0.3 (max) | Not specified | UI | Only specified for 2.5 GT/s. |
| TRX-MIN-PULSE | Minimum width pulse at Rx | Not specified | 0.6 (min) | UI | Measured to account for worst Tj at 10-12 BER. |
| VRX-MAX-MIN-RATIO | min/max pulse voltage on consecutive UI | Not specified | 5 (max) | -- | Rx eye must simultaneously meet VRX\_EYE limits. |
| BWRX-PLL-HI | Maximum Rx PLL bandwidth | 22 (max) | 16 (max) | MHz | Second order PLL jitter transfer bounding function . See Note 3. |
| BWRX-PLL-LO-3DB | Minimum Rx PLL BW for 3 dB peaking | 1.5 (min) | 8 (min) | MHz | Second order PLL jitter transfer bounding function. See Note 3. |
| BWRX-PLL-LO-1DB | Minimum Rx PLL BW for 1 dB peaking | Not specified | 5 (min) | MHz | Second order PLL jitter transfer bounding function. See Note 3. |
| PKGRX-PLL1 | Rx PLL peaking with 8 MHz min BW | Not specified | 3.0 | dB | Second order PLL jitter transfer bounding function . See Note 3. |
| PKGRX-PLL2 | Rx PLL peaking with 5 MHz min BW | Not specified | 1.0 | dB | Second order PLL jitter transfer bounding function. See Note 3. |
| RLRX-DIFF | Rx package plus Si differential return loss | 10 (min) | 10 (min) for 0.05 - 1.25 GHz  8 (min) for 1.25 - 2.5 GHz | dB | See Note 4. |
| RLRX-CM | Common mode Rx return loss | 6 (min) | 6 (min) | dB | See Note 4. |
| ZRX-DC | Receiver DC common mode impedance | 40 (min)  60 (max) | 40 (min)  60 (max) | Ω | DC impedance limits are needed to guarantee Receiver detect. See Note 5. |
| ZRX-DIFF-DC | DC differential impedance | 80 (min)  120 (max) | Not specified | Ω | For 5.0 GT/s covered under RLRX-DIFF parameter. See Note 5. |
| VRX-CM-AC-P | Rx AC common mode voltage | 150 (max) | 150 (max) | mVP | Measured at Rx pins into a pair of 50 Ω terminations into ground. See Note 6. |
| ZRX-HIGH-IMP-DCPOS | DC Input CM Input Impedance for V>0 during Reset or power down | 50 k (min) | 50 k (min) | Ω | Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 – 200 mV with respect to ground. See Note 7. |
| ZRX-HIGH-IMP-DCNEG | DC Input CM Input Impedance for V<0 during Reset or power down | 1.0 k (min) | 1.0 k (min) | Ω | Rx DC CM impedance with the Rx terminations not powered, measured over the range -150 – 0 mV with respect to ground. See Note 7. |
| VRX-IDLE-DETDIFFp-p | Electrical Idle Detect Threshold | 65 (min)  175 (max) | 65 (min)  175 (max) | mV | VRX-IDLE-DET-DIFFp-p = 2\*|VRX-D+ - VRXD-|. Measured at the package pins of the Receiver. |
| TRX-IDLE-DET-DIFFENTERTIME | Unexpected Electrical Idle Enter Detect Threshold Integration Time | 10 (max) | 10 (max) | ms | An unexpected Electrical Idle (VRXDIFFp-p < VRX-IDLE-DET-DIFFp-p) must be recognized no longer than TRX-IDLEDET-DIFF-ENTERTIME to signal an unexpected idle condition. |
| LRX-SKEW | Lane to Lane skew | 20 (max) | 8 (max) | ns | Across all Lanes on a Port. This includes variation in the length of a SKP Ordered Set at the Rx as well as any delay differences arising from the interconnect itself. See Note 8. |
| **Notes** | 1. Receiver eye margins are defined into a 2 x 50 Ω reference load.  2. The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.  3. Two combinations of PLL BW and peaking are specified at 5.0 GT/s to permit designers to make tradeoffs between the two parameters. If the PLL's min BW is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's min BW is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met. Note: a PLL BW extends from zero up to the value(s) defined as the min or max in the above table. For 2.5 GT/s a single PLL bandwidth and peaking value of 1.5-22 MHz and 3.0 dB are defined.  4. Measurements must be made for both common mode and differential return loss. In both cases the DUT must be powered up and DC isolated, and its D+/D- inputs must be in the low-Z state.  5. The Rx DC Common Mode Impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately and the Rx Common Mode Impedance (constrained by RLRX-CM to 50 Ω ±20%) must be within the specified range by the time Detect is entered.  6. Common mode peak voltage is defined by the expression: max{|(Vd+ - Vd-) - V-CMDC|}.  7. ZRX-HIGH-IMP-DC-NEG and ZRX-HIGH-IMP-DC-POS are defined respectively for negative and positive voltages at the input of the Receiver. Transmitter designers need to comprehend the large difference between >0 and <0 Rx impedances when designing Receiver detect circuits.  8. The LRX-SKEW parameter exists to handle repeaters that regenerate Refclk and introduce differing numbers of skips on different Lanes. | | | | |